CLAIMS:

1. An operational amplifier connected to first and second transistors of an H-bridge for sinking and sourcing current, the operational amplifier having a differential input and an output and comprising:

a transconductance circuit connected to receive the differential input and provide an output, wherein the output is connected to the second transistor of the H-bridge;

a gain circuit connected to receive the output from the transconductance circuit, wherein the gain circuit includes a transistor that is matched to the second transistor of the H-bridge;

a buffer circuit connected between the gain circuit and the first transistor of the H-bridge;

a first feedback network comprising:

a level shift circuit connected to the output of the operational amplifier; and

a clamping circuit connected between the level shift circuit and an input of the buffer circuit; and

a second feedback network comprising:

a level shift circuit connected to the output of the operational amplifier; and

a clamping circuit connected between the level shift circuit and the first transistor of the H-bridge.

2. The operational amplifier of claim 1 and further comprising a compensation circuit connected between an output of the gain circuit and the transconductance circuit.

3. The operational amplifier of claim 2 wherein the compensation circuit is a capacitor.

4. The operational amplifier of claim 1 wherein the transconductance circuit is a current mirror output transconductance amplifier.

5. The operational amplifier of claim 1 wherein the gain circuit is a common source amplifier.

6. The operational amplifier of claim 1 wherein the buffer circuit is a source follower circuit.

7. The operational amplifier of claim 1 wherein the clamping circuit of the first feedback network clamps the buffer circuit in order to bias the first transistor of the H-bridge slightly below a threshold voltage when the operational amplifier is sinking current.

8. The operational amplifier of claim 1 wherein the clamping circuit of the second feedback network minimizes the resistance of the second transistor of the H-bridge during a saturation condition.

9. The operational amplifier of claim 1 wherein the operational amplifier is implemented as an integrated circuit (IC).

10. A voice coil motor control circuit for controlling current through a voice coil motor, the control circuit comprising:

first and second input signal nodes for receiving input signals;

first and second voice coil motor nodes for connection to the voice coil motor;

an H-bridge circuit comprising:

a first transistor having a conduction path connected between a first voltage supply node and the first voice coil motor node, the first transistor further having a control region for controlling conduction through the conduction path;

a second transistor having a conduction path connected between the first voltage supply node and the second voice coil motor node, the second transistor further having a control region for controlling conduction through the conduction path;

a third transistor having a conduction path connected between the first voice coil motor node and a second voltage supply node, the third transistor further having a control region for controlling conduction through the conduction path; and

a fourth transistor having a conduction path connected between the second voice coil motor node and the second voltage supply node, the fourth transistor further having a control region for controlling conduction through the conduction path;

a first power amplifier circuit comprising:

an operational amplifier connected to the first voice coil motor node and the control regions of the first and third transistors; and

a feedback network connected to the first and second input signal nodes and the operational amplifier; and

a second power amplifier circuit comprising:

an operational amplifier connected to the second voice coil motor node and the control regions of the second and fourth transistors; and

a feedback network connected to the first and second input signal nodes and the operational amplifier.

11. The control circuit of claim 10 wherein each of the transistors are NDMOS transistors having a source, a drain, a gate and a body, wherein the source is connected to the body, the conduction path is between the drain and the source, and the gate is the control region.

12. The control circuit of claim 10 wherein the feedback network of the first power amplifier is connected to the first and second input signal nodes with the opposite polarity as the feedback network of the second power amplifier.

13. The control circuit of claim 10 wherein each of the feedback networks is a resistive feedback circuit for setting the gain and output voltage of the corresponding power amplifier.

14. The control circuit of claim 10 wherein the operational amplifier of the first power amplifier circuit comprises:

a transconductance circuit connected to receive a differential input from the feedback network of the first power amplifier circuit and provide an output, wherein the output is connected to the control region of the second transistor of the H-bridge circuit;

a gain circuit connected to receive the output from the transconductance circuit, wherein the gain circuit includes a transistor that is matched to the second transistor of the H-bridge circuit;

a buffer circuit connected between the gain circuit and the control region of the first transistor of the H-bridge circuit;

a first feedback network comprising:

a level shift circuit connected to an output of the operational amplifier; and

a clamping circuit connected between the level shift circuit and an input of the buffer circuit; and

a second feedback network comprising:

a level shift circuit connected to the output of the operational amplifier; and

a clamping circuit connected between the level shift circuit and the control region of the first transistor of the H-bridge circuit.

15. The control circuit of claim 14 and further comprising a compensation circuit connected between an output of the gain circuit and the transconductance circuit.

16. The control circuit of claim 15 wherein the compensation circuit is a capacitor.

17. The control circuit of claim 14 wherein the transconductance circuit is a current mirror output transconductance amplifier.

18. The control circuit of claim 14 wherein the gain circuit is a common source amplifier.

19. The control circuit of claim 14 wherein the buffer circuit is a source follower circuit.

20. The control circuit of claim 14 wherein the clamping circuit of the first feedback network clamps the buffer circuit in order to bias the first transistor of the H-bridge circuit slightly below a threshold voltage when the operational amplifier of the first power amplifier circuit is sinking current.

21. The control circuit of claim 14 wherein the clamping circuit of the second feedback network minimizes the resistance of the second transistor of the H-bridge circuit during a saturation condition.

22. The control circuit of claim 10 wherein the control circuit is implemented as an integrated circuit (IC).